

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity And32 is

Port ( x : in STD\_LOGIC;

y : in STD\_LOGIC;

z : out STD\_LOGIC);

end And32;

architecture Behavioral of And32 is

begin

z<= x AND y;

end Behavioral;